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A p.c.m sound-in-syncs distribution system:

synchronization of analogue-to-digital and digital-to-analogue converters to television line frequency

No. 1969/44

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

RESEARCH DEPARTMENT

A P.C.M. SOUND-IN-SYNCS DISTRIBUTION SYSTEM: SYNCHRONIZATION OF ANALOGUE-TO-DIGITAL AND DIGITAL-TO-ANALOGUE CONVERTERS TO TELEVISION LINE FREQUENCY

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(EL-33)

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SUMMARY

Audio analogue-to-digital and digital-to-analogue converters (a.d.c.s and d.a.c.s) of the ramp-counter type, designed initially to run from crystal-controlled clocks, have been modified for use in conjunction with the sound-in-syncs distribution system described in Report 1969/35. To this end it was necessary to synchronize the converter operation with television line frequencies, which are subject to erratic variations, and to take steps to minimise disturbances through non-synchronous switching between picture sources.

The modified converters will synchronize to any 625 line 50 field picture source and during four months of field trials and demonstrations in several locations have required neither adjustment nor repair.

1. INTRODUCTION

In the sound-in-syncs distribution system described in Report 1969/35, the sound component of a television programme is carried by p.c.m. signals accommodated in the line sync pulse period. It was therefore necessary that the associated analogue-to-digital converter (a.d.c.) be synchronized to the television line frequency.

Television line frequency as originated by numerous and sometimes widely-separated picture sources is necessarily somewhat variable. Mean line-frequency errors of about 1 part in 10^4 occur together with line jitter which may be up to $\pm$ 1 μs.

A.d.c.s and d.a.c.s as previously designed for high-quality sound signals and described in Report EL-18 were driven by crystal-controlled clocks and could not be synchronized to television line frequencies having the errors described above. This report describes how the converters were modified to synchronize to television and also a further modification to avoid ill effects caused by non-synchronous switching between picture sources.

2. GENERAL

In Report EL-18 various methods of analogue-to-digital and digital-to-analogue conversion are described and it is shown that the ramp-counter type of converter is particularly suitable for the coding and decoding of high-quality sound signals.

Ramp-counter converters operate by measuring out an interval of time proportional to the quantity to be converted and accumulating the output quantity at a fixed rate during that time. In an a.d.c. the time is that required for a ramp voltage to become equal to the signal voltage while the output number is being accumulated in a counter. In a d.a.c. the time is that required for the input number to be counted out while the output voltage is being accumulated by a rising ramp.

The units in which the time interval is measured are complete periods of a stable clock as registered by the counter. The ramp and counter must start simultaneously, otherwise at the end of the time interval the number accumulated in the a.d.c. would be subject to an uncertainty of one count and the ramp height in the d.a.c. similarly subject to a random error of up to one level.

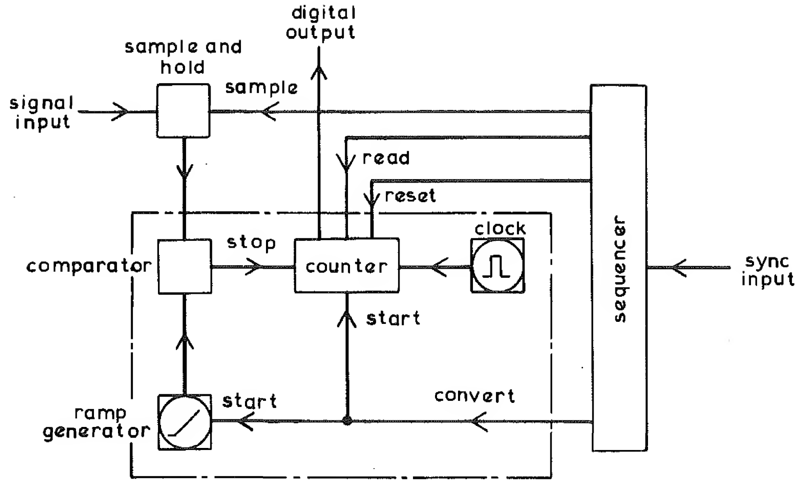

Fig. 1 - Ramp counter a.d.c.

A block diagram of a ramp-counter a.d.c. is given in Fig. 1.

The ramp generator, comparator, counter, and clock units are enclosed in a dotted box. These units comprise the converter proper i.e. they produce the signal in its converted form. The sequencer and the sample and hold unit, which are shown outside the box, provide ancillary services such as presenting a held sample, resetting the ramp and counter, initiating the conversion process when all is ready and reading out the answer when conversion is complete. The timing of these ancillary functions is controlled by the sync input.

In the a.d.c. described in Report EL-18 the converter was free-running and the synchronizing input to the sequencer was derived by frequency division from the clock, since there was no necessity to synchronize it to an external source. Operation of both sections of the converter from a common clock automatically ensured that the counter and the ramp always started in the required fixed time relationship.

The modifications which are needed to keep the time relationship fixed when the converters are locked to television are described below.

3. METHODS OF SYNCHRONIZATION TO TELEVISION

3.1. Counter Clock Flywheel Synchronized

When it is necessary to synchronize converters using a single clock to an external system, the clock may be flywheel-synchronized to the controlling source, as shown in Fig. 2, only when that source is itself precise in frequency and free from timing jitter. Regrettably this requirement is met only by the most stable colour television picture sources, and flywheel synchronization of a.d.c.s is therefore inapplicable to most video signals.

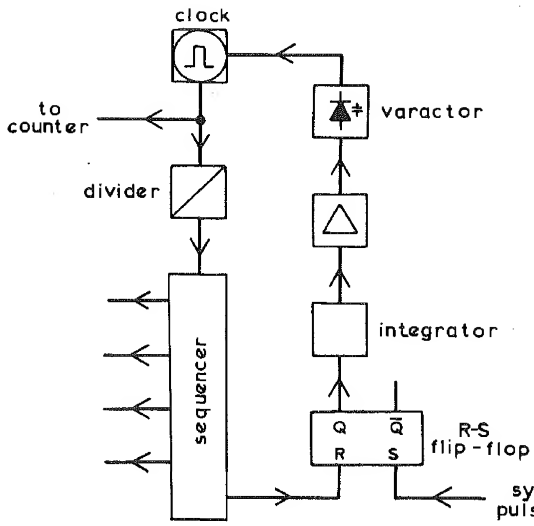

Fig. 2 - Flywheel synchronization of counter clock

To synchronize the converter to television it is preferable to separate the ancillary functions of the converting equipment from the counting function, hard-locking the former to the video waveform and leaving the latter under the control of a separate fixed-frequency clock.

3.2. Counter Clock Triggered by the Line Syncs

The necessary fixed time relationship between ramp start and counter start could, in principle, be ensured if the counter clock were stopped after the completion of each conversion and started again in a fixed phase by a 'convert' command pulse from the sequencer. The problems of triggering the high-speed clock into immediate equilibrium operation are, however, formidable and this solution was not attempted.

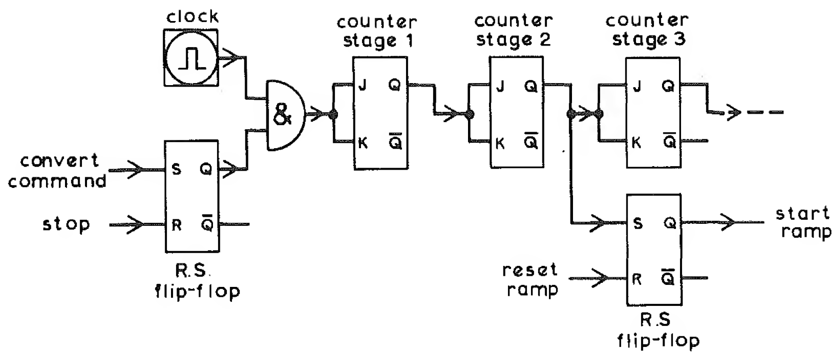

Fig. 3 - Ramp-starting logic for a.d.c.

3.3. Counter Clock Output Gated by Line Syncs

If the high-speed clock is allowed to run free and without interruption there will be a random phase relationship between the 'convert' command pulse and the clock. The 'convert' command pulse cannot in these circumstances be used to start the ramp, as this would make the starting of the ramp, and hence the eventual moment of equality of the ramp and signal voltages, uncertain in time with respect to the clock. In the present equipment the 'convert' command pulse is therefore arranged to gate the output from the clock to the counter, and the counter, by starting, in turn starts the ramp. Fig. 3 shows a schematic of the ramp-starting logic of the analogue-to-digital converter. It will be noticed that the 'start ramp' signal is derived from the first transition of the output of 2nd counter stage. The reason for this is that on those occasions when the 'convert' command occurs during a clock pulse, the gate may mutilate the first pulse applied to the counter; the transition of the output of the counter stage may in turn be slowed down, and the timing of the start ramp pulse become uncertain. The second counter stage however operates on the second effective clock pulse, the leading edge of which is never sliced by the gate, and a precisely timed start for the ramp is therefore assured. By this means a small loss in signal-to-noise ratio is avoided, and although the a.d.c. cannot now produce the first coded level, the proportion of the encodable range thus sacrificed – one part in 2048 for an 11 bit a.d.c. – is clearly negligible.

In the d.a.c., for which the ramp-starting logic is shown in Fig. 4, incoming digits are pre-set into the counter before conversion begins. The second counter stage cannot be used to control the ramp start, since the transition time of the second stage depends upon the data set into the first stage. It is necessary to start the ramp at the time of the first transition of the first counter stage irrespective of the direction of that transition; to this end 'and' gates 2 and 3, controlled by the input data, are used to connect the appropriate output of counter stage no. 1 to the ramp starting mechanism.

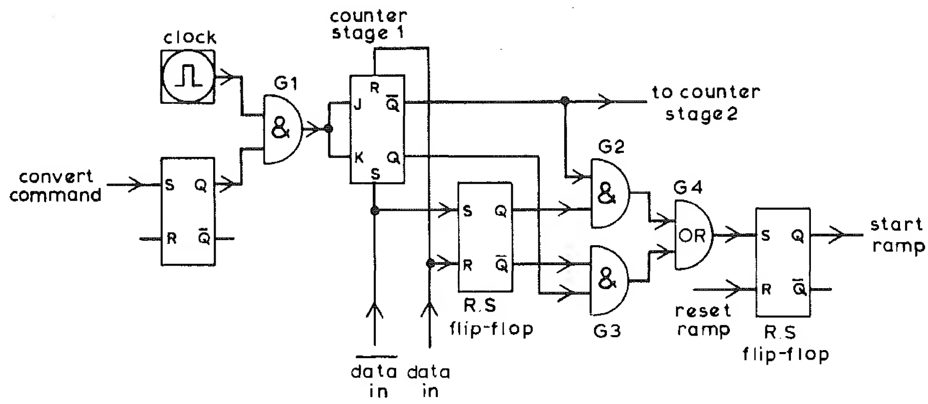

Fig. 4 - Ramp-starting logic for d.a.c.

With this arrangement it is not possible to avoid the small loss in signal-to-noise ratio due to mutilated pulses.

4. PERFORMANCE OF MODIFIED CONVERTERS

Separation of the control of the counting and ancillary functions has permitted the a.d.c. and d.a.c. to operate from television systems in which the line frequency errors may be as high as ± 3%, a tolerance which is ample to deal with all picture sources acceptable for broadcast use.

The signal-to-noise ratios of the a.d.c.-d.a.c. combination obtainable when using all 11 bits* of the code lies within 1 dB of the theoretical value, the experimental accuracy of the measurement being about ± 1 dB. The lack of complete rigour in the ramp starting mechanism of the d.a.c., mentioned in Section 3.3, is thus seen to be of small significance since it, together with all other causes of excess noise, produced little deviation from the theoretical quantizing noise value.

The modifications to the converters outlined in this report have a direct bearing upon the synchronizing and signal-to-noise performance. The remaining performance figures, while not directly affected by the modifications with which this report is chiefly concerned, are given below for completeness.

Table 1 gives the harmonic distortion figures for a 1000 Hz sine-wave signal for an a.d.c.-d.a.c. pair for signal levels ½ dB and 8 dB below the maximum for the system. The distortion present is predominantly 2nd harmonic arising in the analogue circuits; previous experience indicates that this would be inaudible even under critical listening conditions.

TABLE 1

Harmonic No.	HARMONIC PERCENTAGE	
	Input level +7·5 dBm	Input level 0 dBm
2	0·38	0·12
3	0·14	0·045
4	0·025	—
5	0·01	0·015
6	—	—

* For reasons given in an earlier report (1969/35) in this series, only 10 bits were eventually utilized in the experimental sound-in-syncs equipment.

The overall frequency response of an a.d.c. pair is that of a number of nominally flat analogue circuits in cascade plus a sinx/x frequency term due to the spectrum of the rectangular p.a.m. pulses applied to the interpolating filter in the d.a.c. In the present case equalization is applied to remove the sinx/x frequency term and to compensate approximately for any frequency-dependent attenuation in the nominally flat analogue circuits. The frequency response of the coder-decoder pair lies within ± 0·5 dB from 20 Hz to 14 kHz; this figure represents the accuracy with which the equalization within the d.a.c. has been carried out and could readily be improved on to any desired extent.

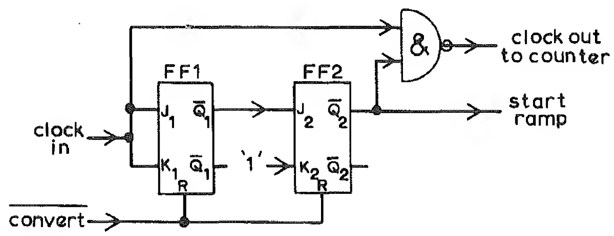

Fig. 5 - Alternative ramp-starting logic for a.d.c.s and d.a.c.s

5. FURTHER POSSIBILITIES

An alternative method of ensuring synchronism of the ramp start and the counter start, which was developed subsequently to the building of the a.d.c.s described above, appears to offer some advantages. The circuit is shown in Fig. 5 and the appropriate timing diagram in Fig. 6. In this arrangement flip/flop F/F1 is used to catch the first clock pulse after the 'convert' command and then to divide by 2. The flip/flop F/F2 driven by the output of F/F1, is used as a latch to release the ramp and start the counter.

The complement of the 'convert' command signal i.e. '$\overline{\text{convert}}$', initially holds the two flip/flops reset. The command to convert releases the flip/flops and and next upward-going edge of the clock signal brings output $\overline{Q}_1$ of F/F1 to 0. The upward edge of the following clock pulse sets $\overline{Q}_2$ to 0. The transition of $\overline{Q}_2$ to 0 releases the short circuit on the ramp and thus starts the ramp; it also opens the nand gate ($\overline{\&}_1$) and the next and subsequent downward clock edges are transmitted as upward-going edges to be counted. It will be seen that the timing of the ramp start and of the first count are unaffected by variations of the position of the transition of the '$\overline{\text{convert}}$' signal within the clock cycle.

This starting system has the advantage of being equally applicable to a.d.c.s and d.a.c.s. It has also the attraction of being rigorously correct even in the case where the first clock pulse applied to F/F1 may

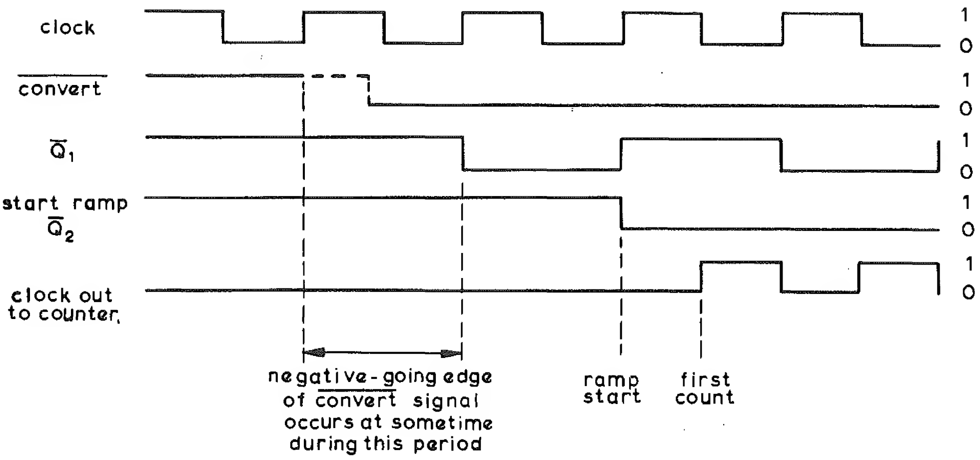

Fig. 6 - Timing diagram for logic of Fig. 5

be sliced by the gating action of the 'convert' command, though its signal-to-noise advantage over the starting techniques actually used in the a.d.c.s and d.a.c.s described above may be small.

6. NON-SYNCHRONOUS PICTURE SWITCHES

The a.d.c.s described in Research Report EL-18 delivered their output in serial form to the television combining equipment and the results of each conversion were erased from the a.d.c. output register immediately after being read out. Failure of the television system to maintain a regular succession of synchronizing pulses to the a.d.c. resulted in lost read-out and transmission of an all-zeros code. This instantaneous excursion to the full-scale value of the output signal produced a loud 'plop' in the sound output.

In the modified a.d.c.s described in this present report, the digital output is retained in the coder output register until the start of the next conversion and information is passed to the television combining equipment in parallel form at a time controlled by the combiner. As a result, failure of the 'convert' command pulse due to non-synchronized picture switching results in repeated reading out of the previously held value until correct working is restored. The error signal energy transmitted and hence the subjective disturbance is thus greatly reduced.

7. CONCLUSION

The modified converters have fulfilled the requirements of the sound-in-syncs system. During four months in which experimental equipment incorporating two a.d.c.s and two d.a.c.s has been on trial in various locations no faults have occurred and no adjustments have been found necessary.

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